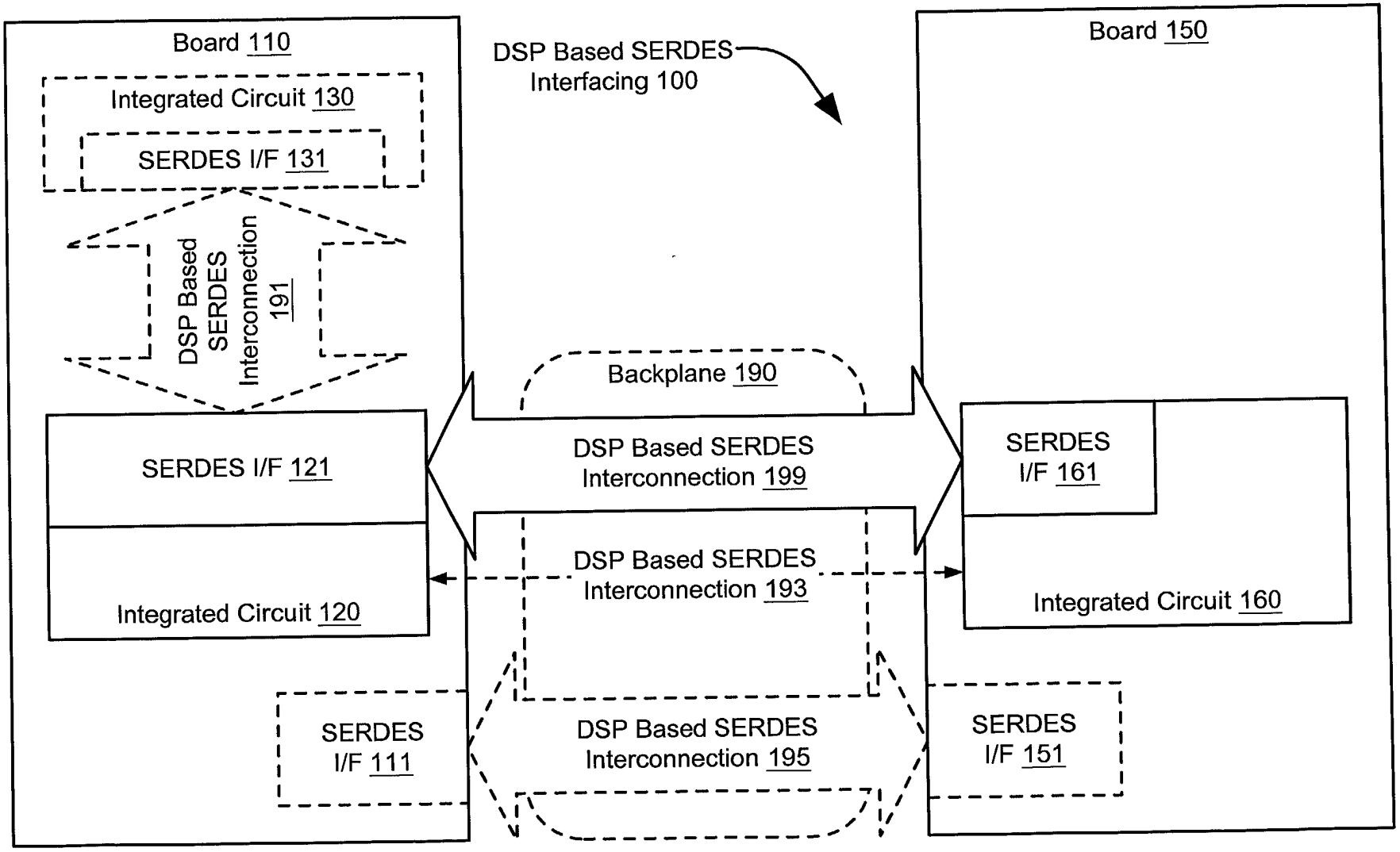

Board 110
Integrated Circuit 130
SERDES I/F 131
DSP Based SERDES Interconnection 191
DSP Based SERDES Interfacing 100
Board 150
Backplane 190
SERDES I/F 121
DSP Based SERDES Interconnection 199
SERDES I/F 161
DSP Based SERDES Interconnection 193
Integrated Circuit 120
Integrated Circuit 160
SERDES I/F 111
DSP Based SERDES Interconnection 195
SERDES I/F 151

Fig. 1

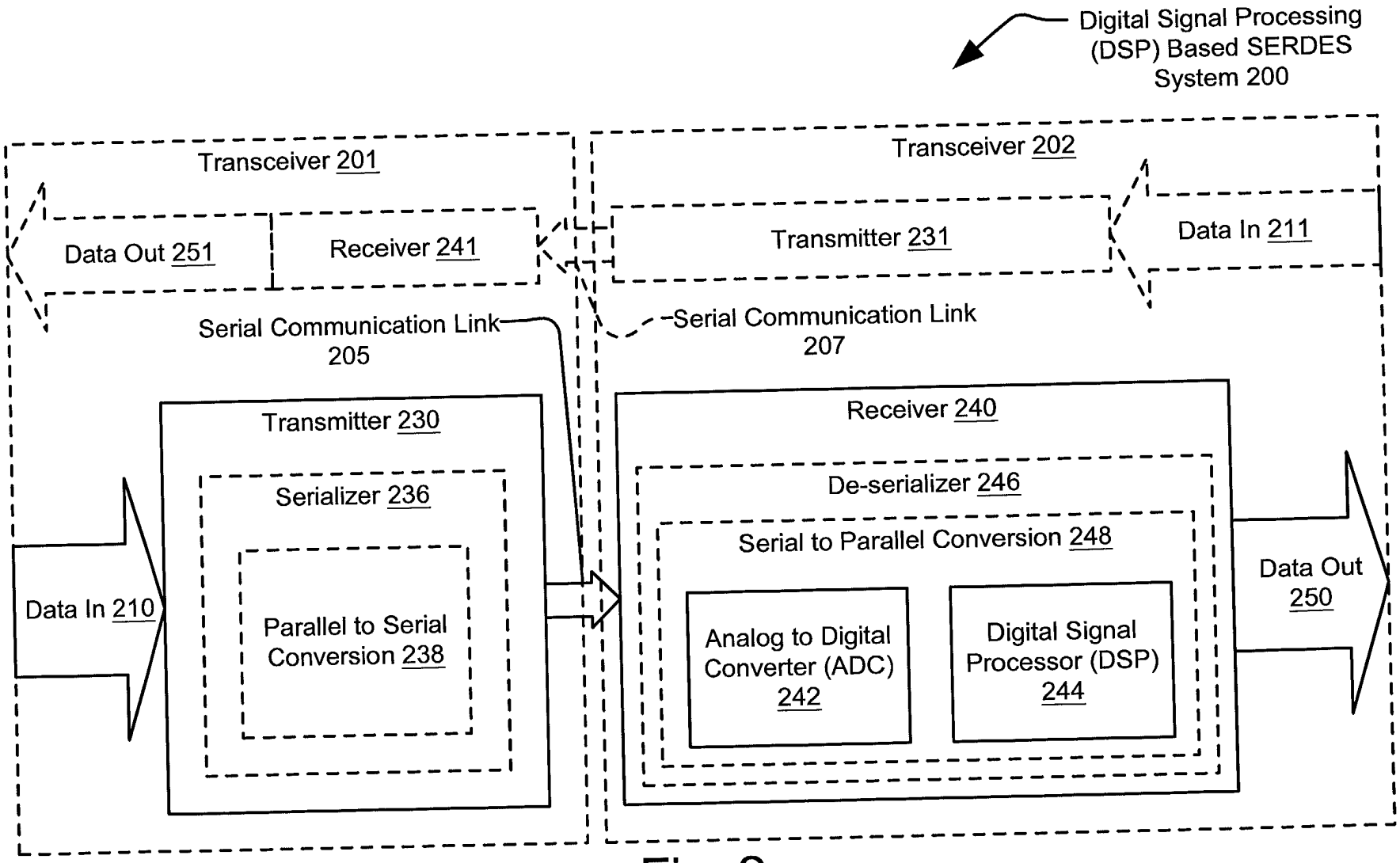

Digital Signal Processing (DSP) Based SERDES System 200
Transceiver 201
Data Out 251
Receiver 241
Serial Communication Link 205
Transmitter 230
Serializer 236
Parallel to Serial Conversion 238
Data In 210
Transceiver 202
Transmitter 231
Data In 211
Serial Communication Link 207
Receiver 240
De-serializer 246
Serial to Parallel Conversion 248
Analog to Digital Converter (ADC) 242
Digital Signal Processor (DSP) 244
Data Out 250

Fig. 2

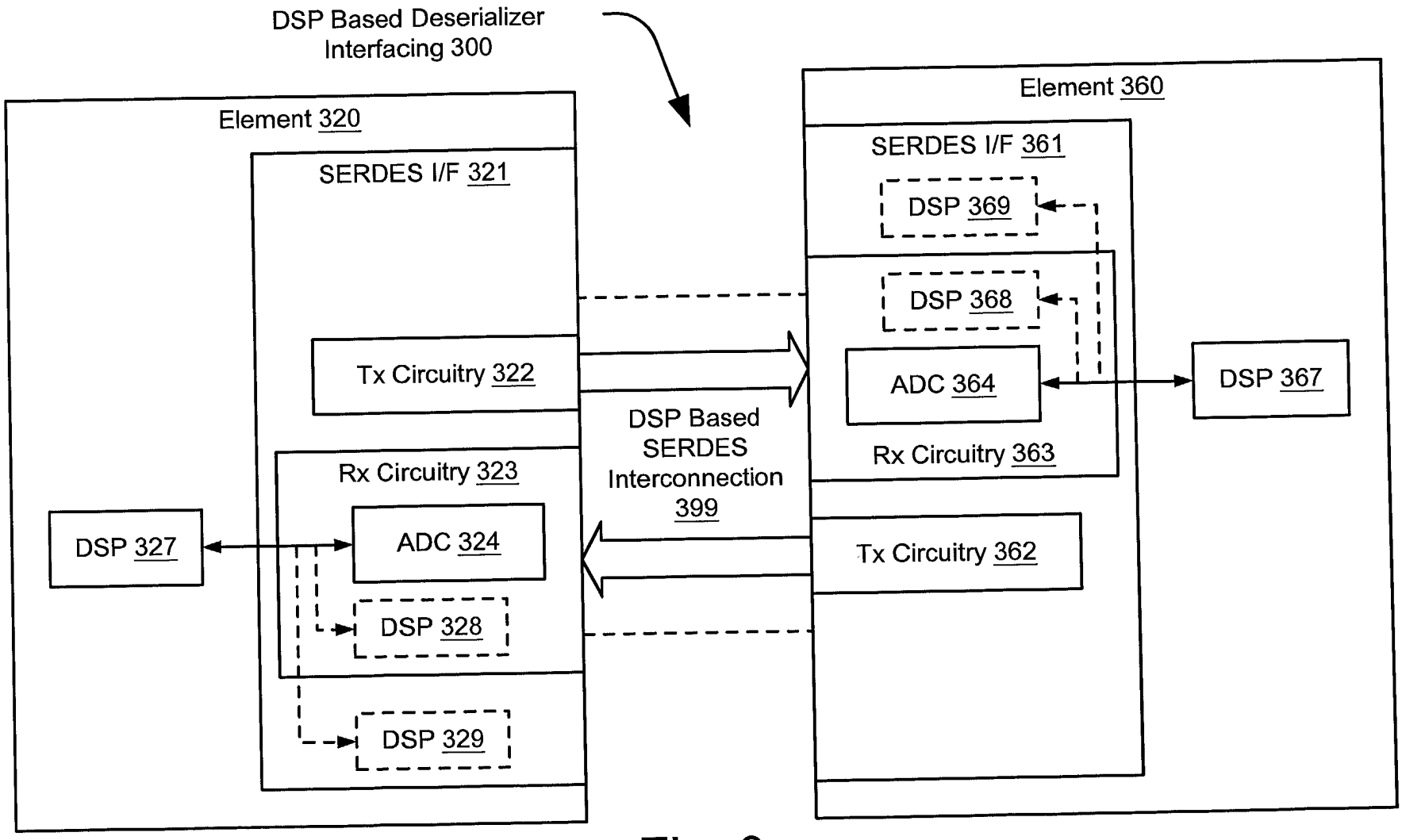

DSP Based Deserializer Interfacing 300
Element 320
SERDES I/F 321
Tx Circuitry 322
Rx Circuitry 323
DSP 327
ADC 324
DSP 328
DSP 329
DSP Based SERDES Interconnection 399
Element 360
SERDES I/F 361
DSP 369
DSP 368
ADC 364
Rx Circuitry 363
DSP 367
Tx Circuitry 362

Fig. 3

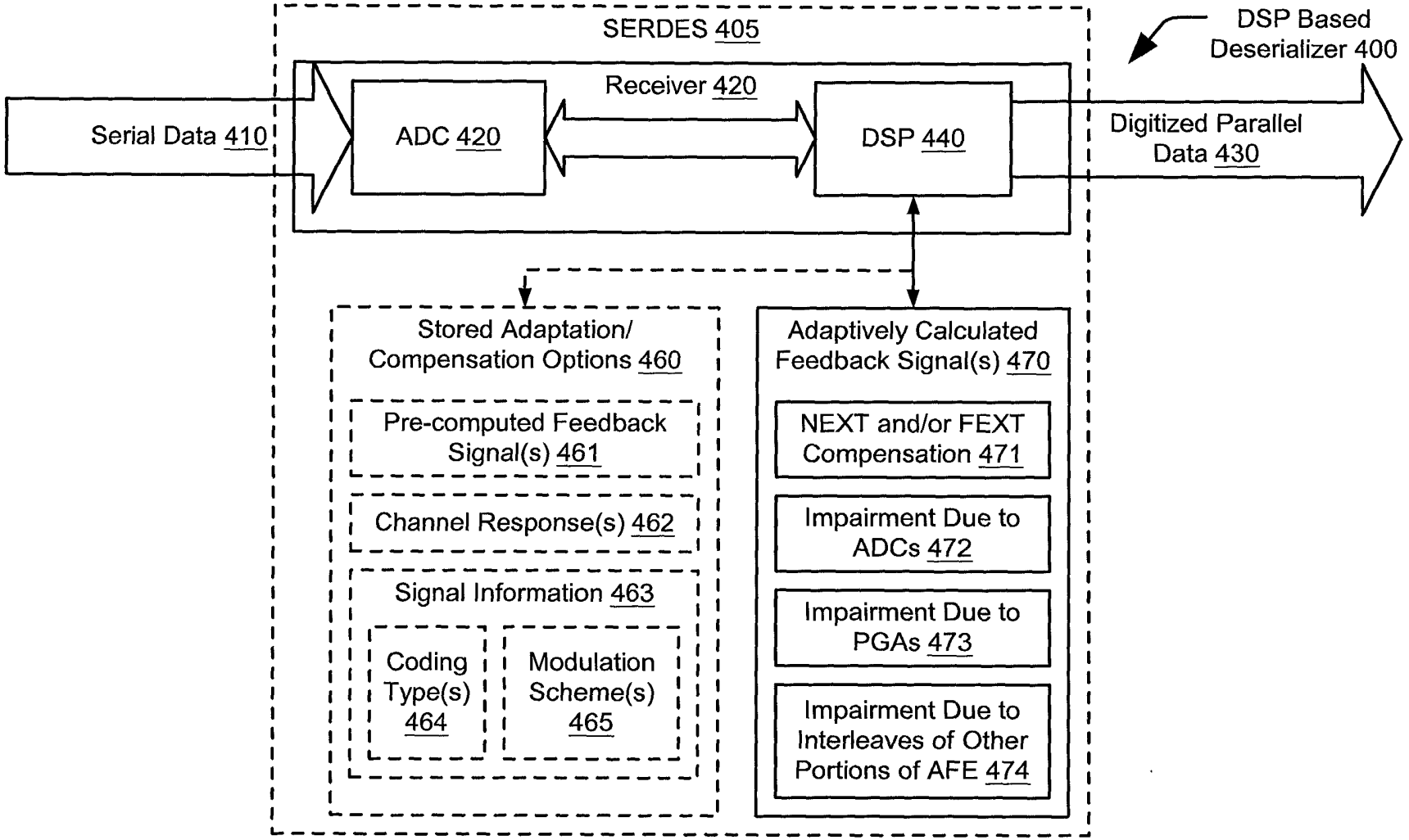

SERDES 405
DSP Based Deserializer 400
Receiver 420
Serial Data 410
ADC 420
DSP 440
Digitized Parallel Data 430
Stored Adaptation/ Compensation Options 460
Pre-computed Feedback Signal(s) 461
Channel Response(s) 462
Signal Information 463
Coding Type(s) 464
Modulation Scheme(s) 465
Adaptively Calculated Feedback Signal(s) 470
NEXT and/or FEXT Compensation 471
Impairment Due to ADCs 472
Impairment Due to PGAs 473
Impairment Due to Interleaves of Other Portions of AFE 474

Fig. 4

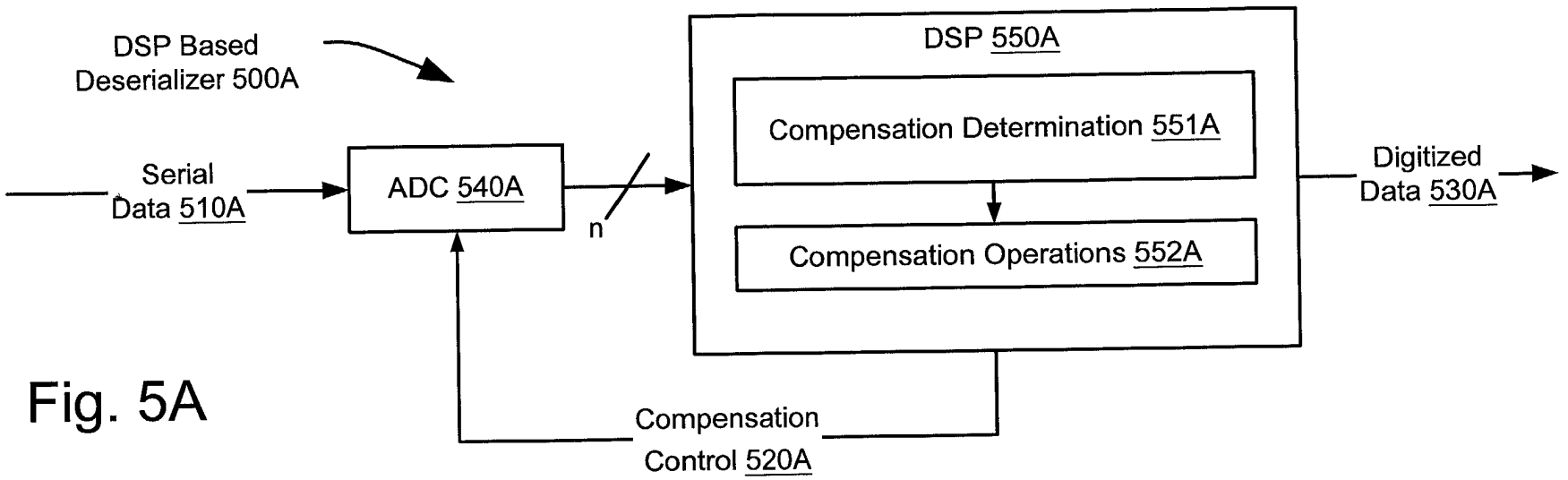

DSP Based
Deserializer 500A
Serial
Data 510A
ADC 540A
n
DSP 550A
Compensation Determination 551A
Compensation Operations 552A
Digitized
Data 530A
Compensation
Control 520A

Fig. 5A

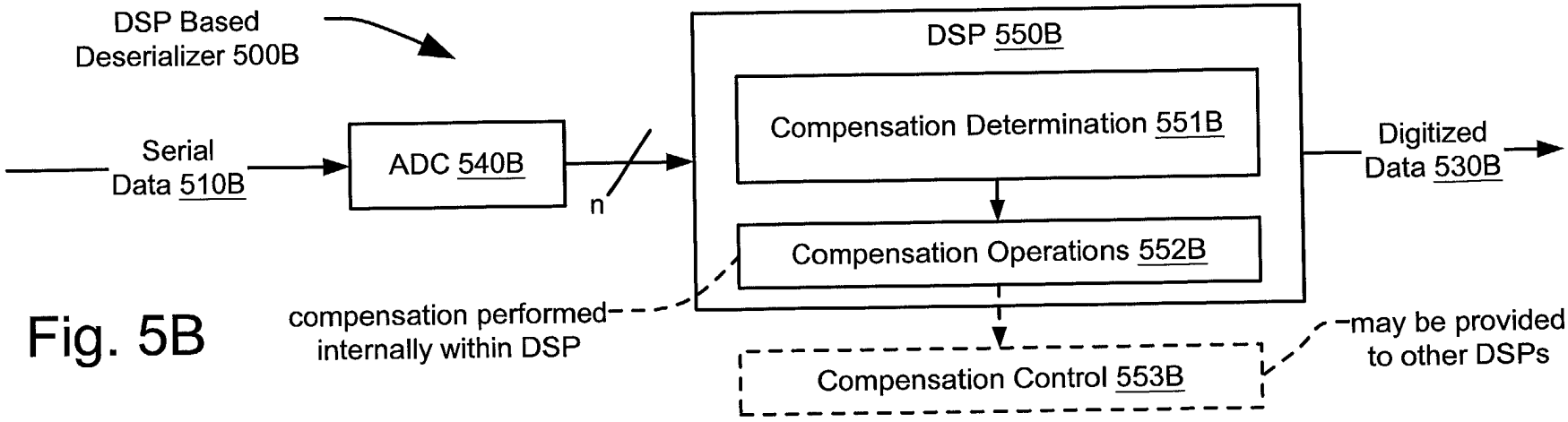

DSP Based
Deserializer 500B
Serial
Data 510B
ADC 540B
n
DSP 550B
Compensation Determination 551B
Compensation Operations 552B
Digitized
Data 530B
compensation performed
internally within DSP
Compensation Control 553B
may be provided
to other DSPs

Fig. 5B

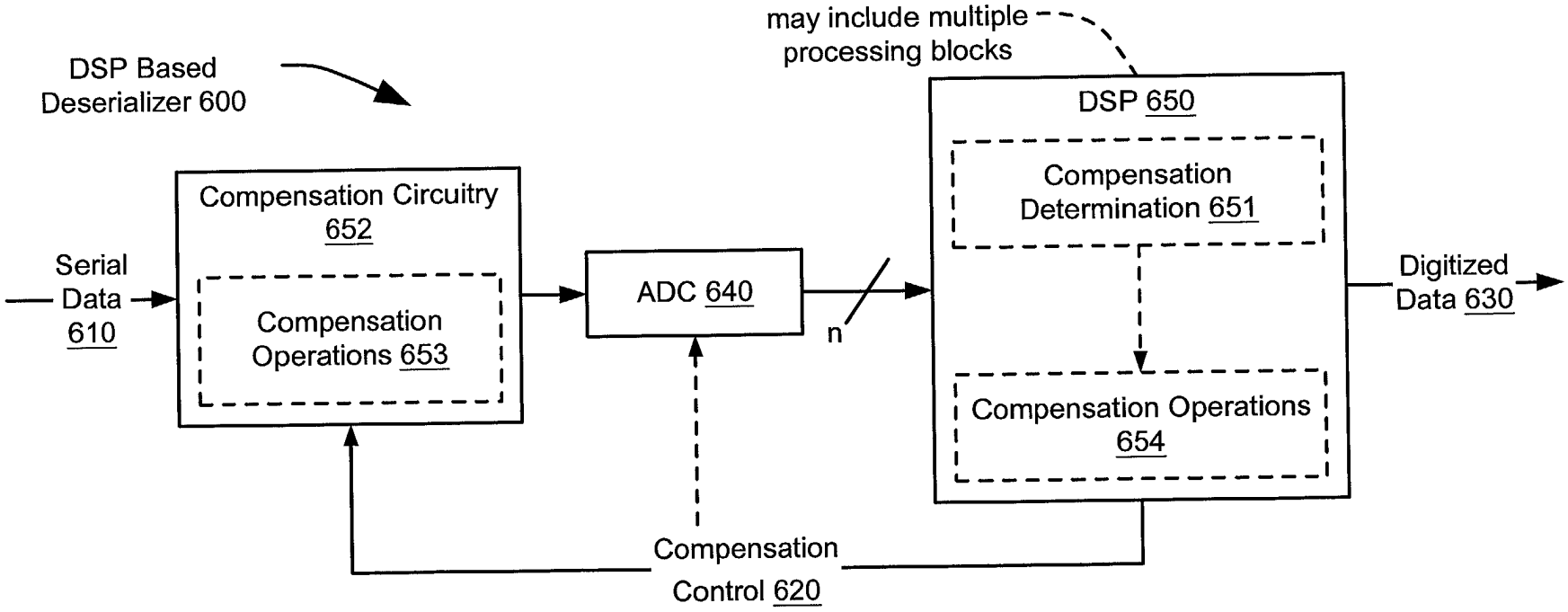

may include multiple processing blocks
DSP Based Deserializer 600
DSP 650
Compensation Determination 651
Compensation Circuitry 652
Serial Data 610
Compensation Operations 653
ADC 640
n
Digitized Data 630
Compensation Operations 654
Compensation Control 620

Fig. 6

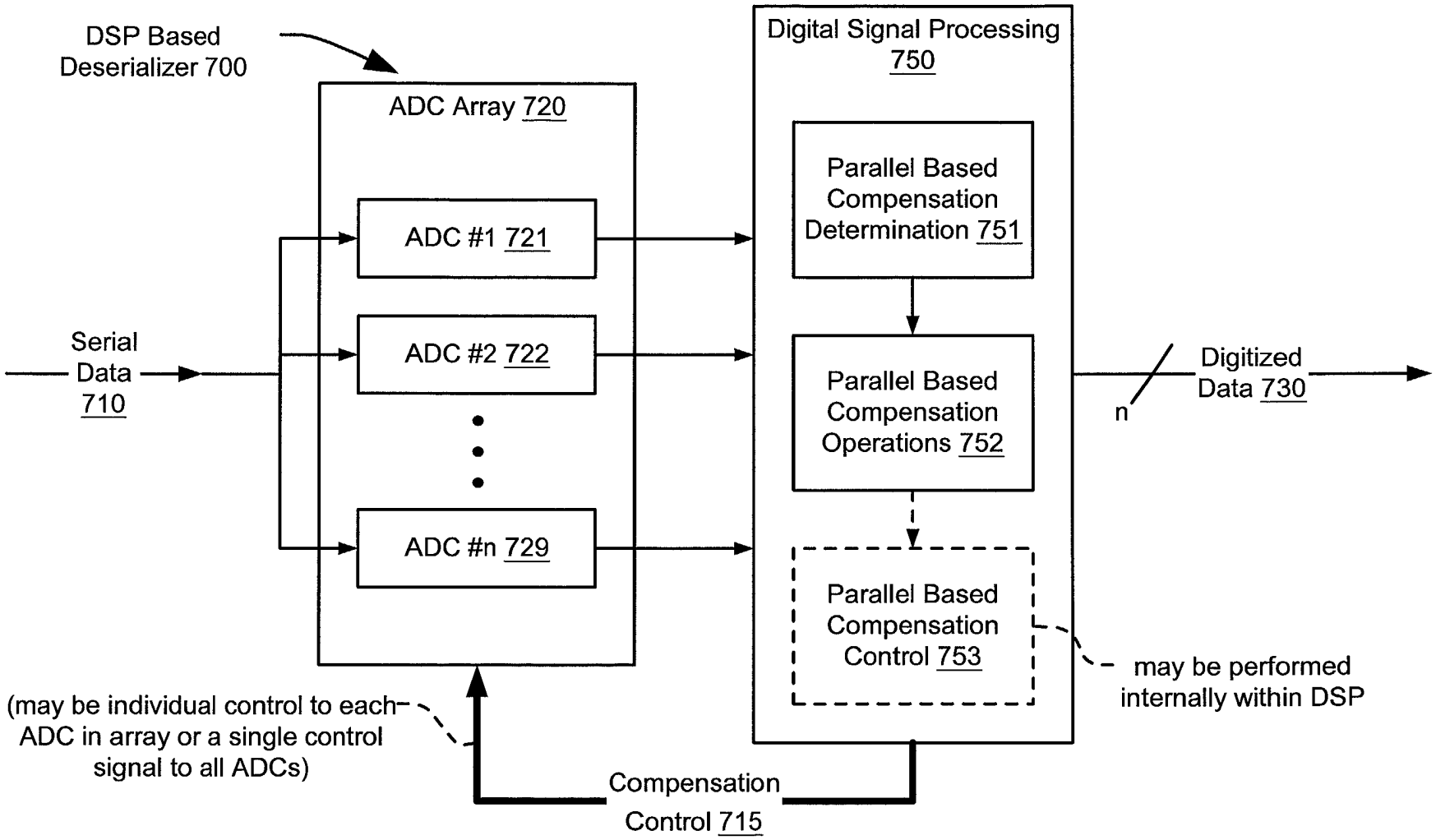

DSP Based
Deserializer 700
ADC Array 720
ADC #1 721
ADC #2 722
ADC #n 729
Serial
Data
710
Digital Signal Processing
750
Parallel Based
Compensation
Determination 751
Parallel Based
Compensation
Operations 752
Parallel Based
Compensation
Control 753
n
Digitized
Data 730
may be performed
internally within DSP
(may be individual control to each
ADC in array or a single control
signal to all ADCs)
Compensation
Control 715

Fig. 7

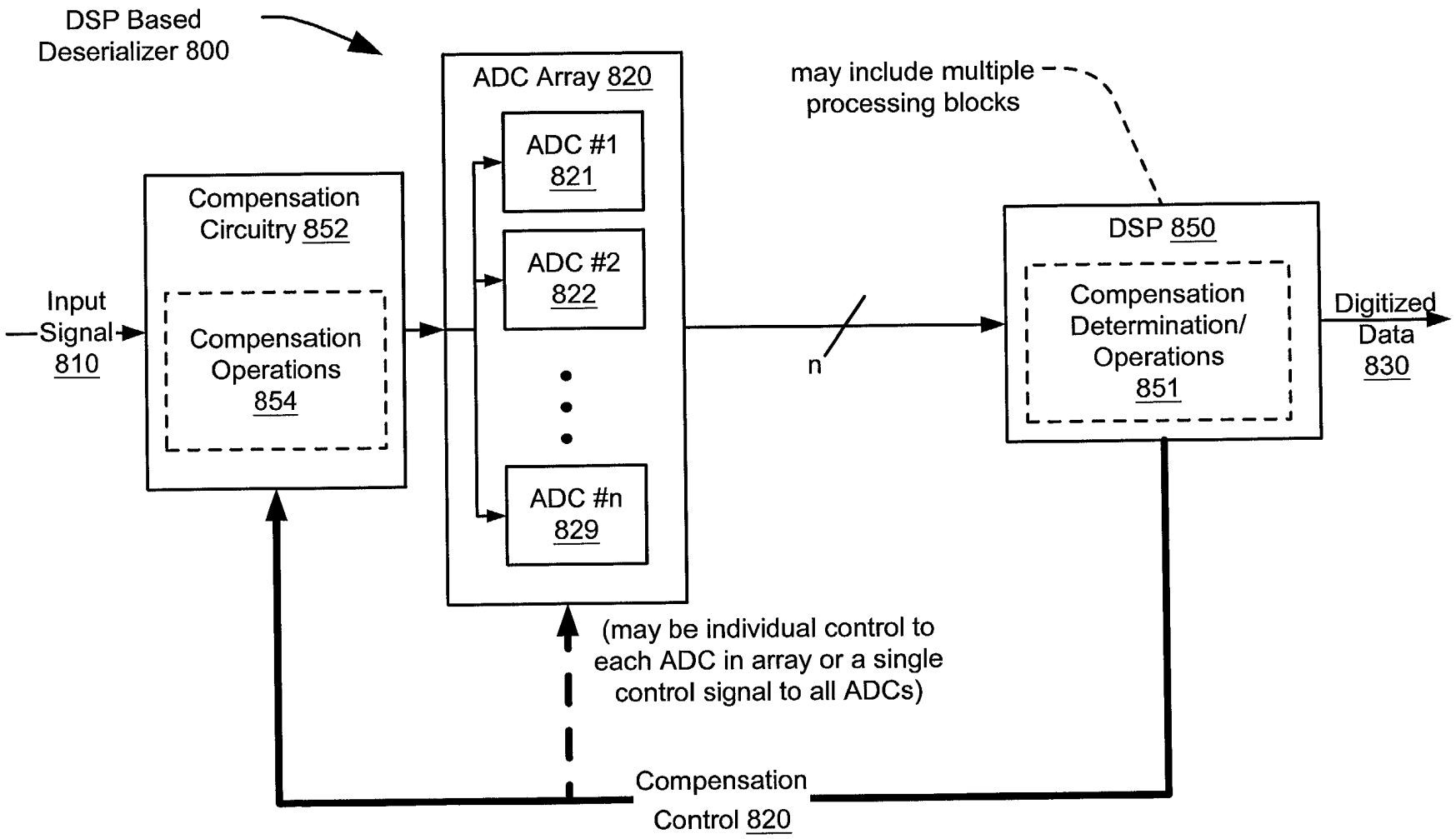

DSP Based
Deserializer 800
ADC Array 820
may include multiple
processing blocks
ADC #1
821
ADC #2
822
ADC #n
829
Compensation
Circuitry 852
Compensation
Operations
854
Input
Signal
810
n
DSP 850
Compensation
Determination/
Operations
851
Digitized
Data
830
(may be individual control to
each ADC in array or a single
control signal to all ADCs)
Compensation
Control 820

Fig. 8

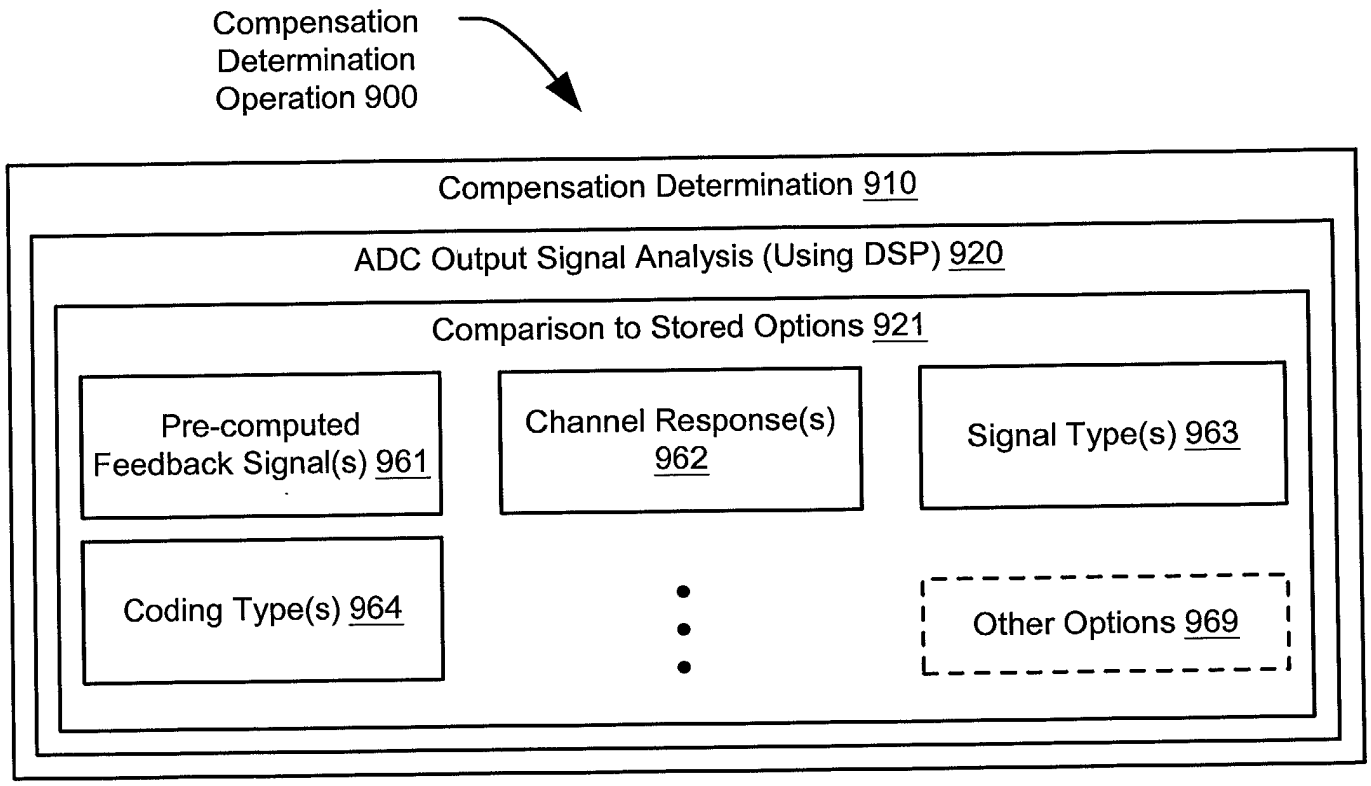

Compensation Determination Operation 900
Compensation Determination 910
ADC Output Signal Analysis (Using DSP) 920
Comparison to Stored Options 921
Pre-computed Feedback Signal(s) 961
Channel Response(s) 962
Signal Type(s) 963
Coding Type(s) 964
Other Options 969

Fig. 9

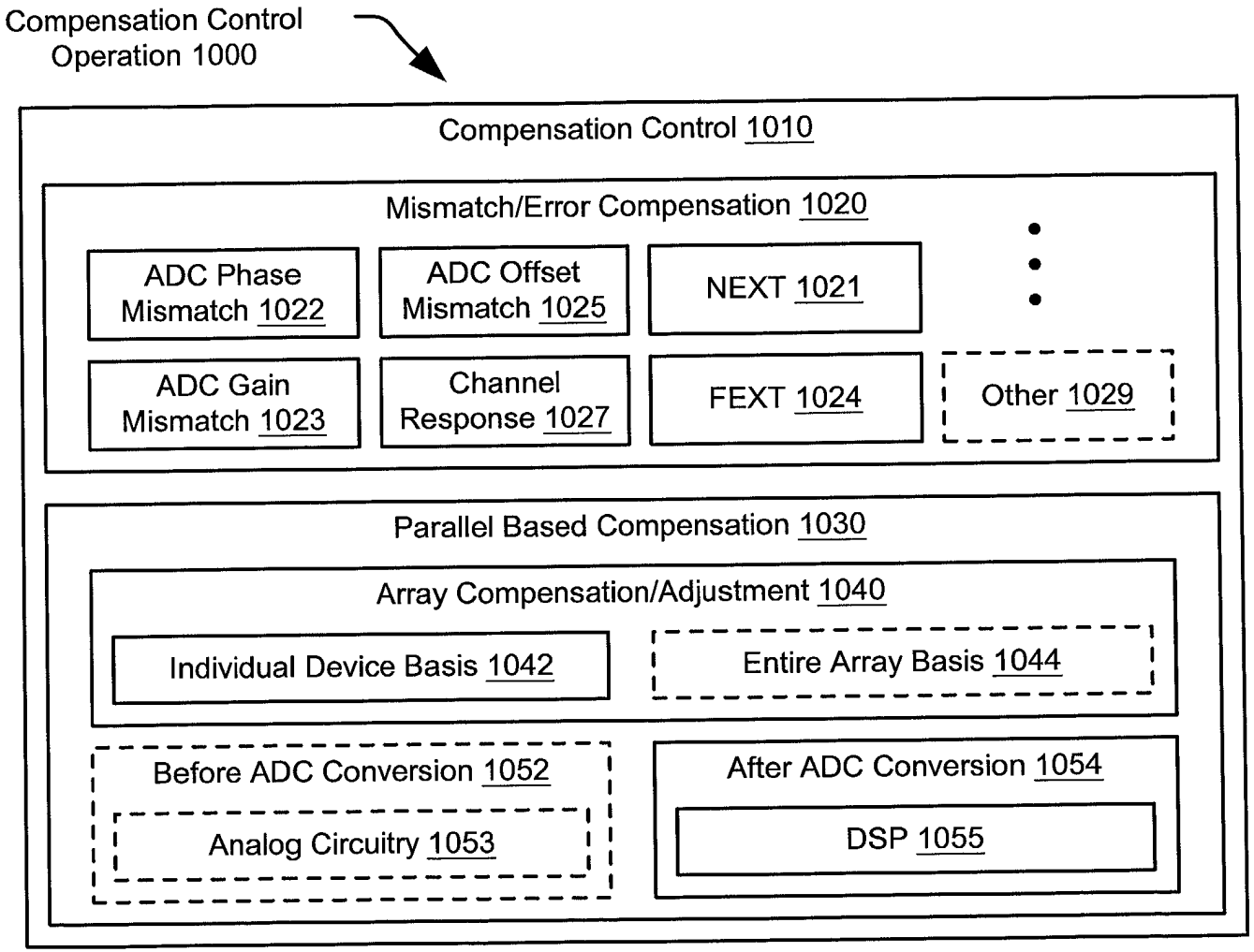

Compensation Control Operation 1000
Compensation Control 1010
Mismatch/Error Compensation 1020
ADC Phase Mismatch 1022
ADC Offset Mismatch 1025
NEXT 1021
ADC Gain Mismatch 1023
Channel Response 1027
FEXT 1024
Other 1029
Parallel Based Compensation 1030
Array Compensation/Adjustment 1040
Individual Device Basis 1042
Entire Array Basis 1044
Before ADC Conversion 1052
Analog Circuitry 1053
After ADC Conversion 1054
DSP 1055

Fig. 10

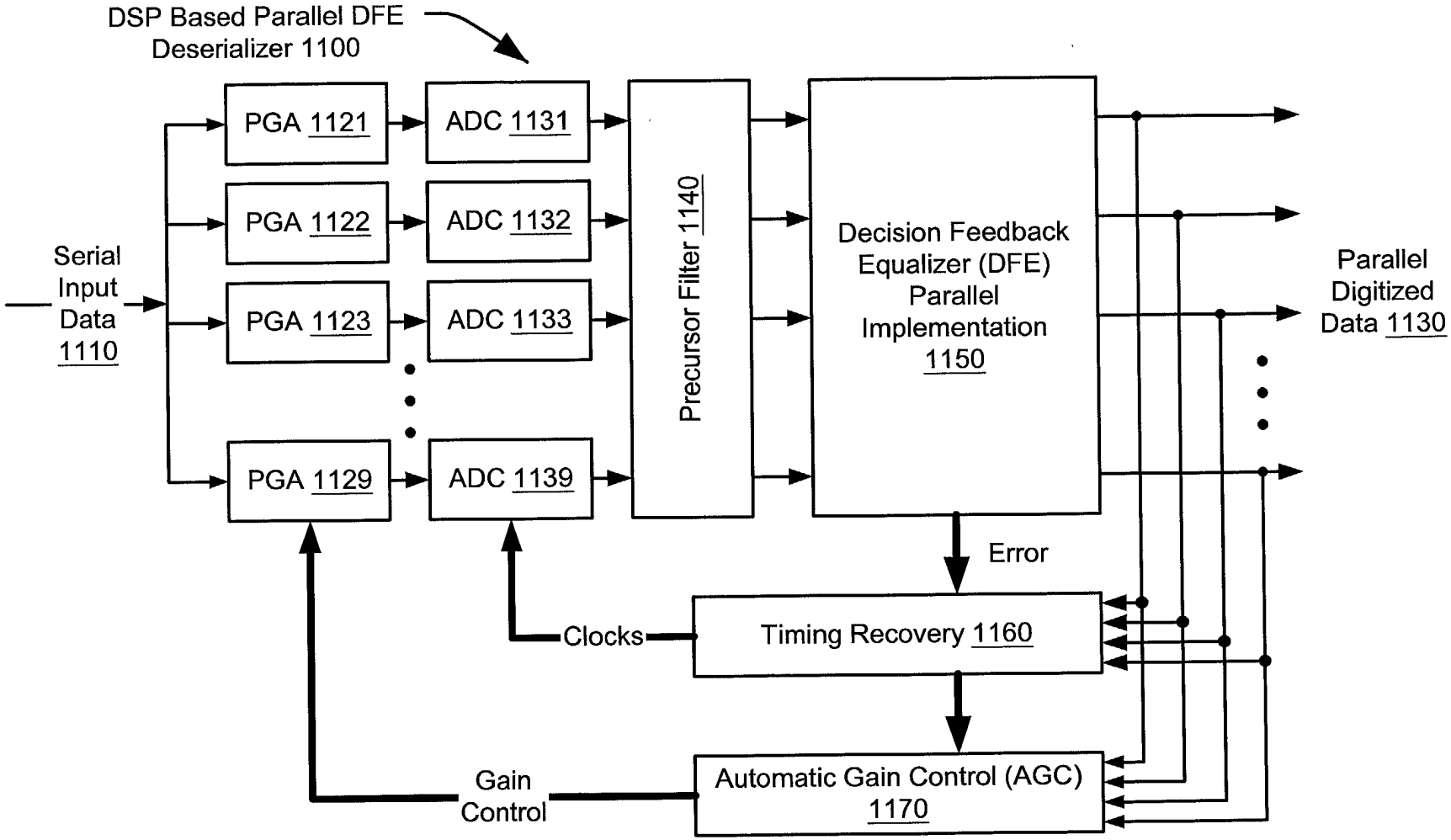

DSP Based Parallel DFE
Deserializer 1100
Serial
Input
Data
1110
PGA 1121
PGA 1122
PGA 1123
PGA 1129
ADC 1131
ADC 1132
ADC 1133
ADC 1139
Precursor Filter 1140
Decision Feedback
Equalizer (DFE)
Parallel
Implementation
1150
Parallel
Digitized
Data 1130
Error
Clocks
Timing Recovery 1160
Gain
Control
Automatic Gain Control (AGC)
1170

Fig. 11

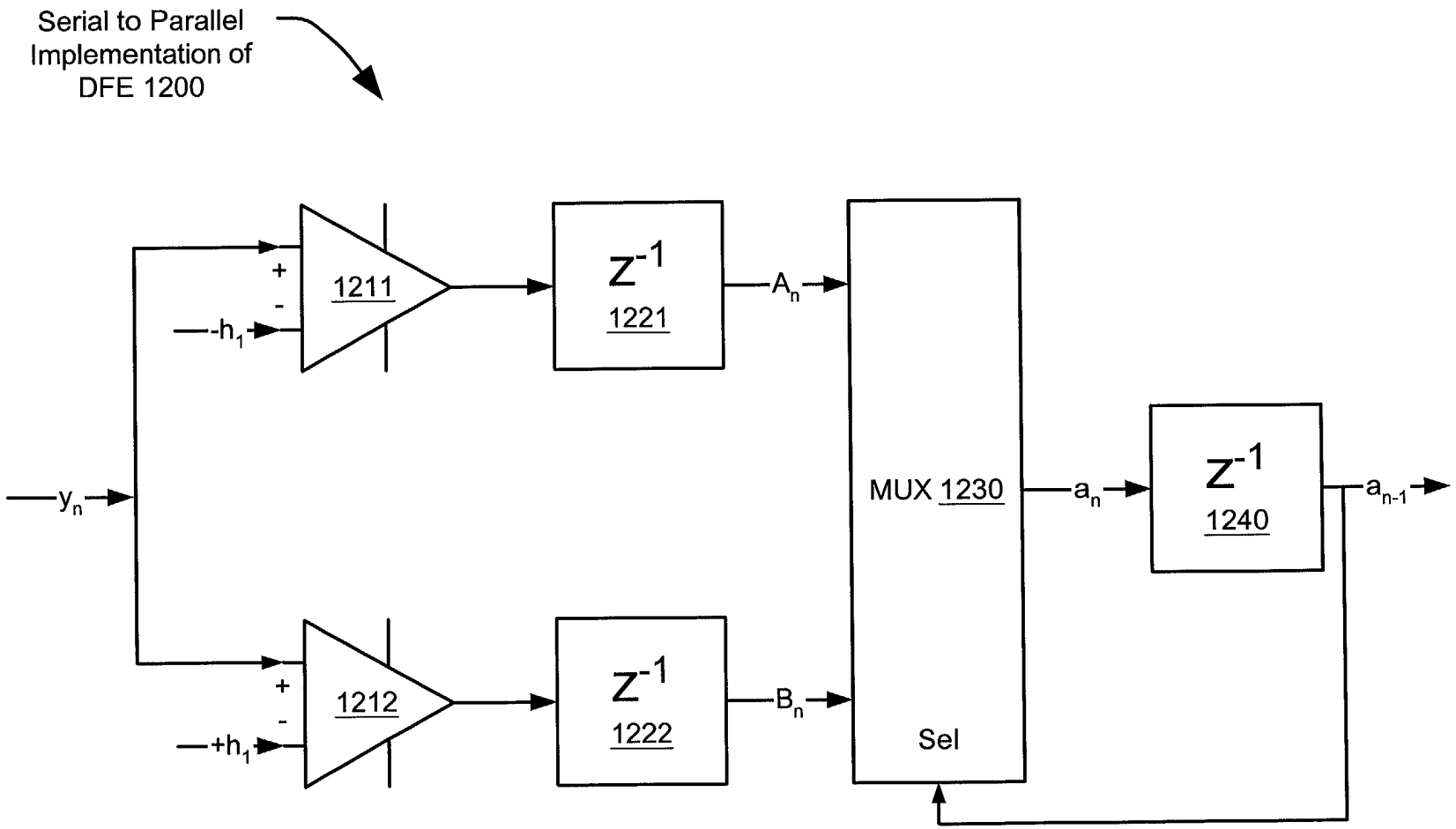

Serial to Parallel Implementation of DFE 1200
1211
+
-
-h1
Z-1
1221
An
MUX 1230
Sel
an
Z-1
1240
an-1
yn
1212
+
-
+h1
Z-1
1222
Bn

Fig. 12

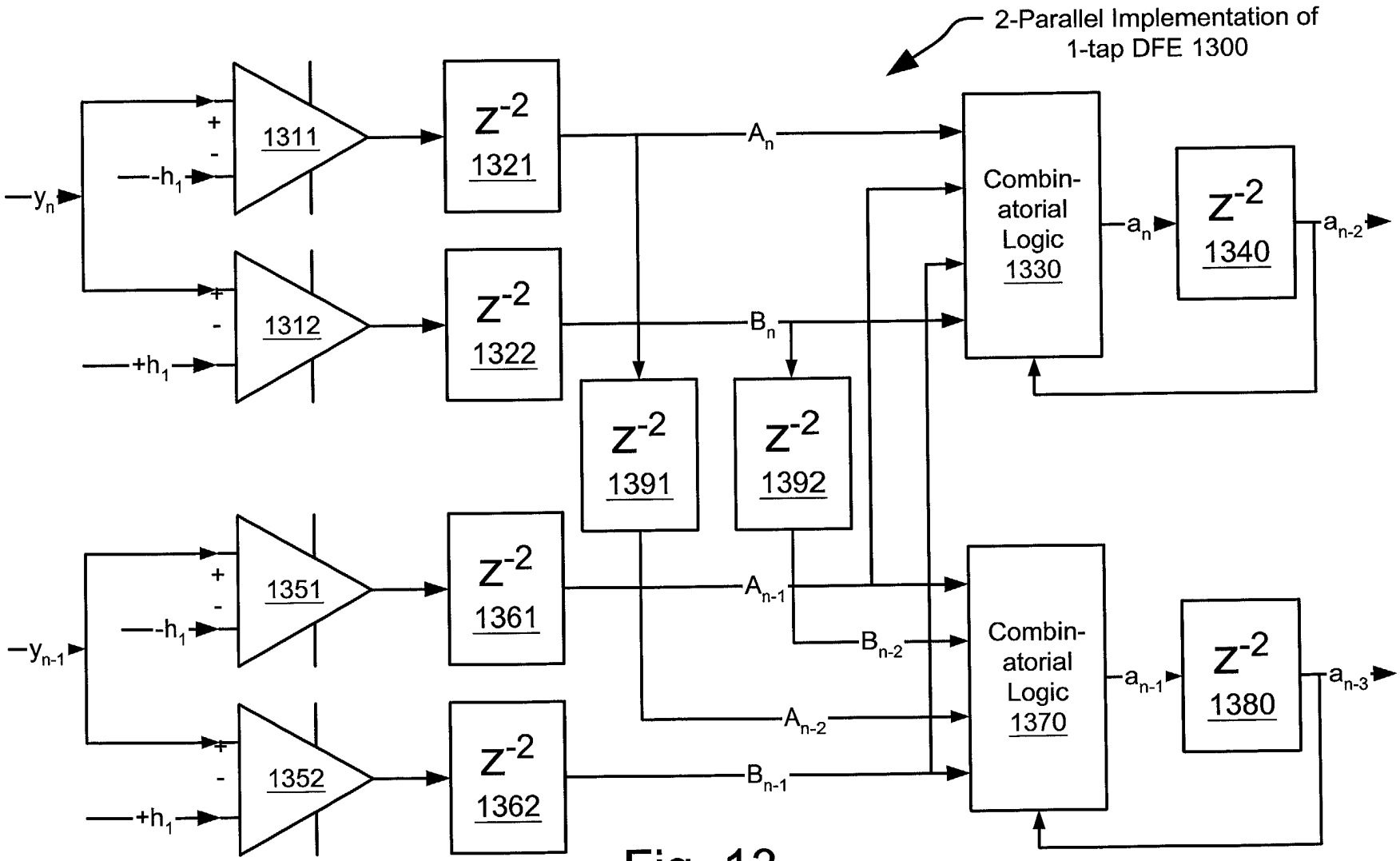

2-Parallel Implementation of
1-tap DFE 1300
1311
1312
1321
1322
1330
1340
1351
1352
1361
1362
1370
1380
1391
1392
z^{-2}
y_n
y_{n-1}
$-h_1$
$+h_1$
A_n
B_n
A_{n-1}
B_{n-2}
A_{n-2}
B_{n-1}
a_n
a_{n-2}
a_{n-1}
a_{n-3}
Combin-
atorial
Logic

Fig. 13

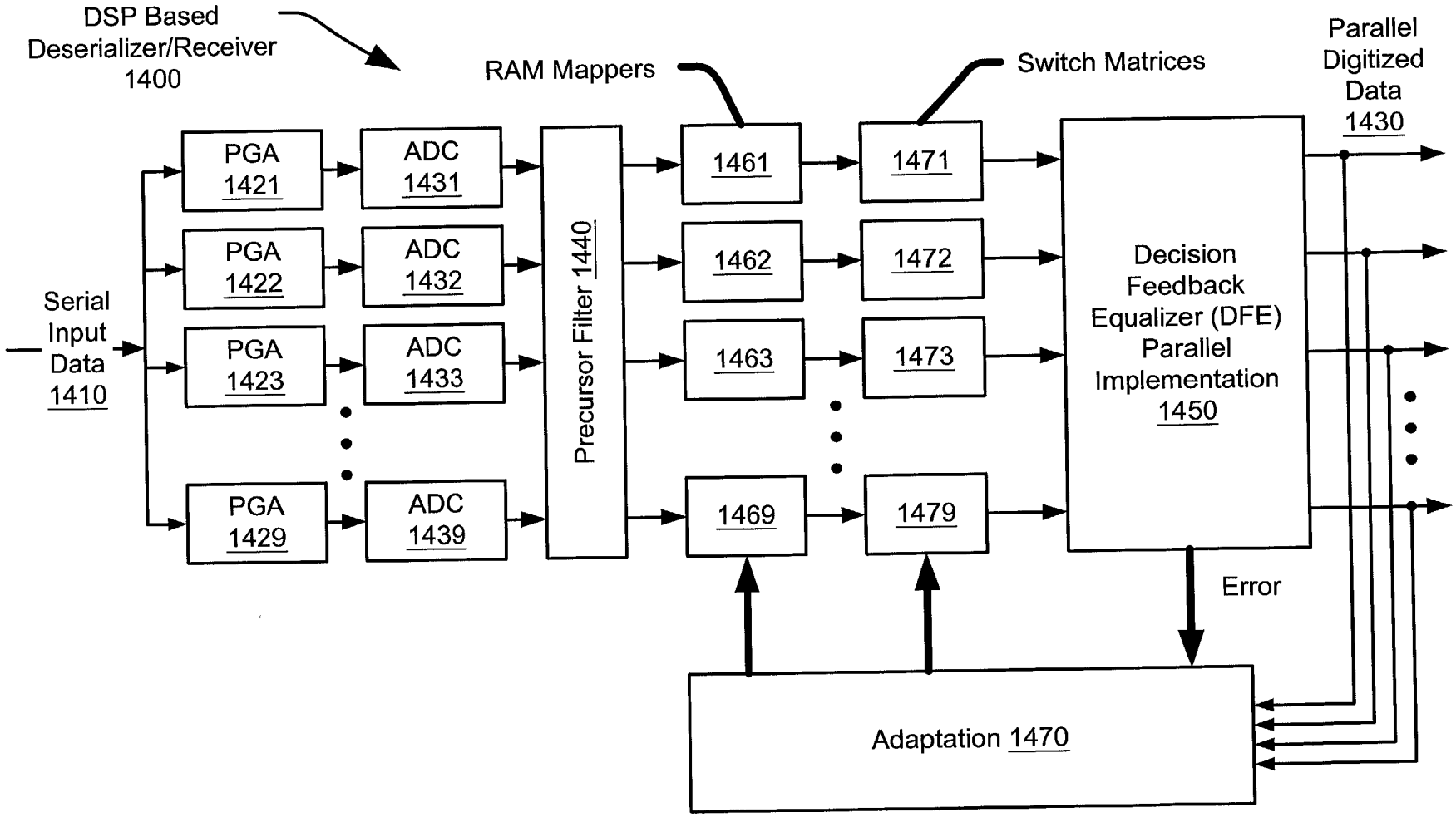

DSP Based
Deserializer/Receiver
1400
RAM Mappers
Switch Matrices
Parallel
Digitized
Data
1430
Serial
Input
Data
1410
PGA
1421
PGA
1422
PGA
1423
PGA
1429
ADC
1431
ADC
1432
ADC
1433
ADC
1439
Precursor Filter 1440
1461
1462
1463
1469
1471
1472
1473
1479
Decision
Feedback
Equalizer (DFE)
Parallel
Implementation
1450
Error
Adaptation 1470

Fig. 14

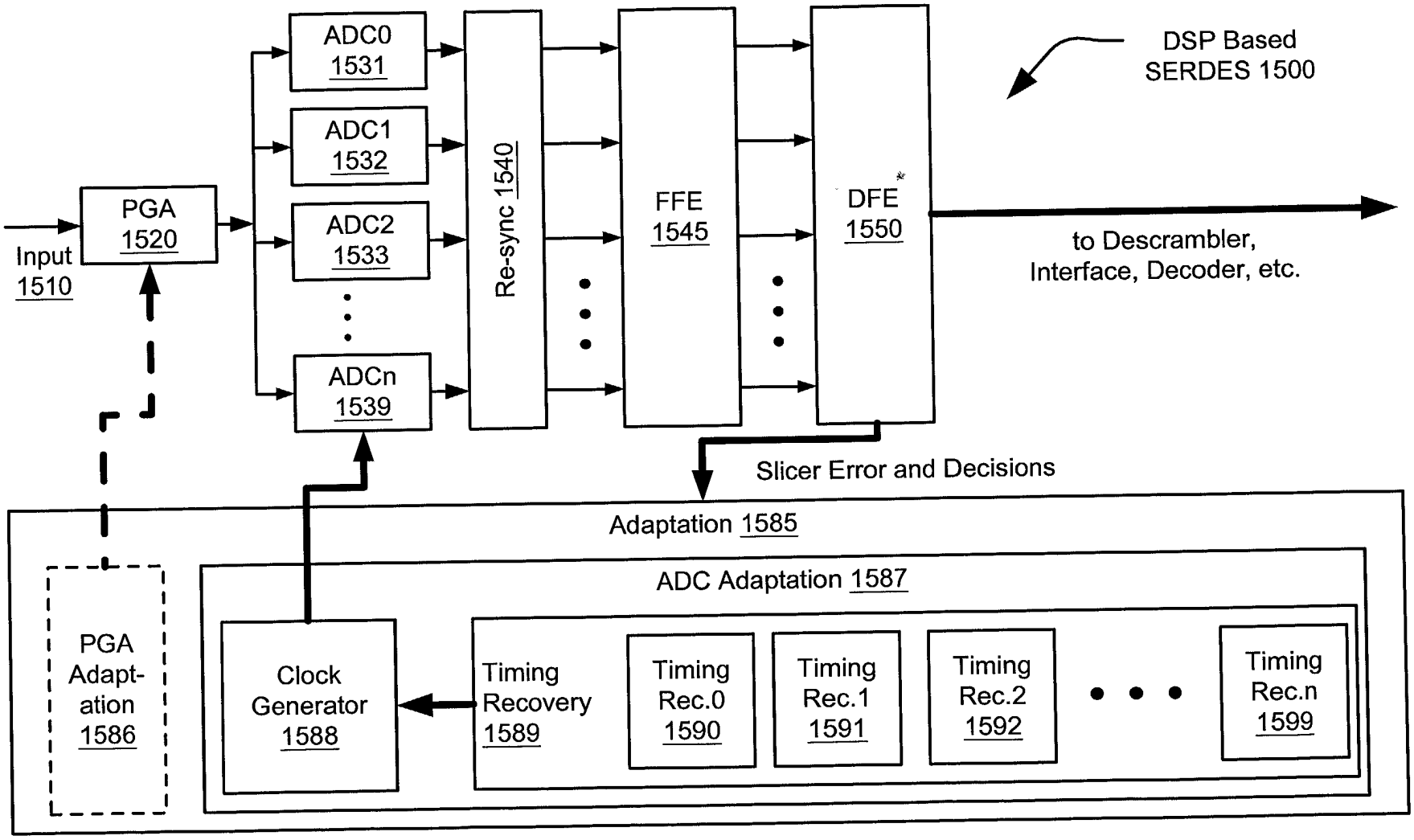

ADC0
1531
ADC1
1532
ADC2
1533
ADCn
1539
Re-sync 1540
FFE
1545
DFE
1550
DSP Based
SERDES 1500
PGA
1520
Input
1510
to Descrambler,
Interface, Decoder, etc.
Slicer Error and Decisions
Adaptation 1585
ADC Adaptation 1587
PGA
Adapt-
ation
1586
Clock
Generator
1588
Timing
Recovery
1589
Timing
Rec.0
1590
Timing
Rec.1
1591
Timing
Rec.2
1592
Timing
Rec.n
1599

Fig. 15

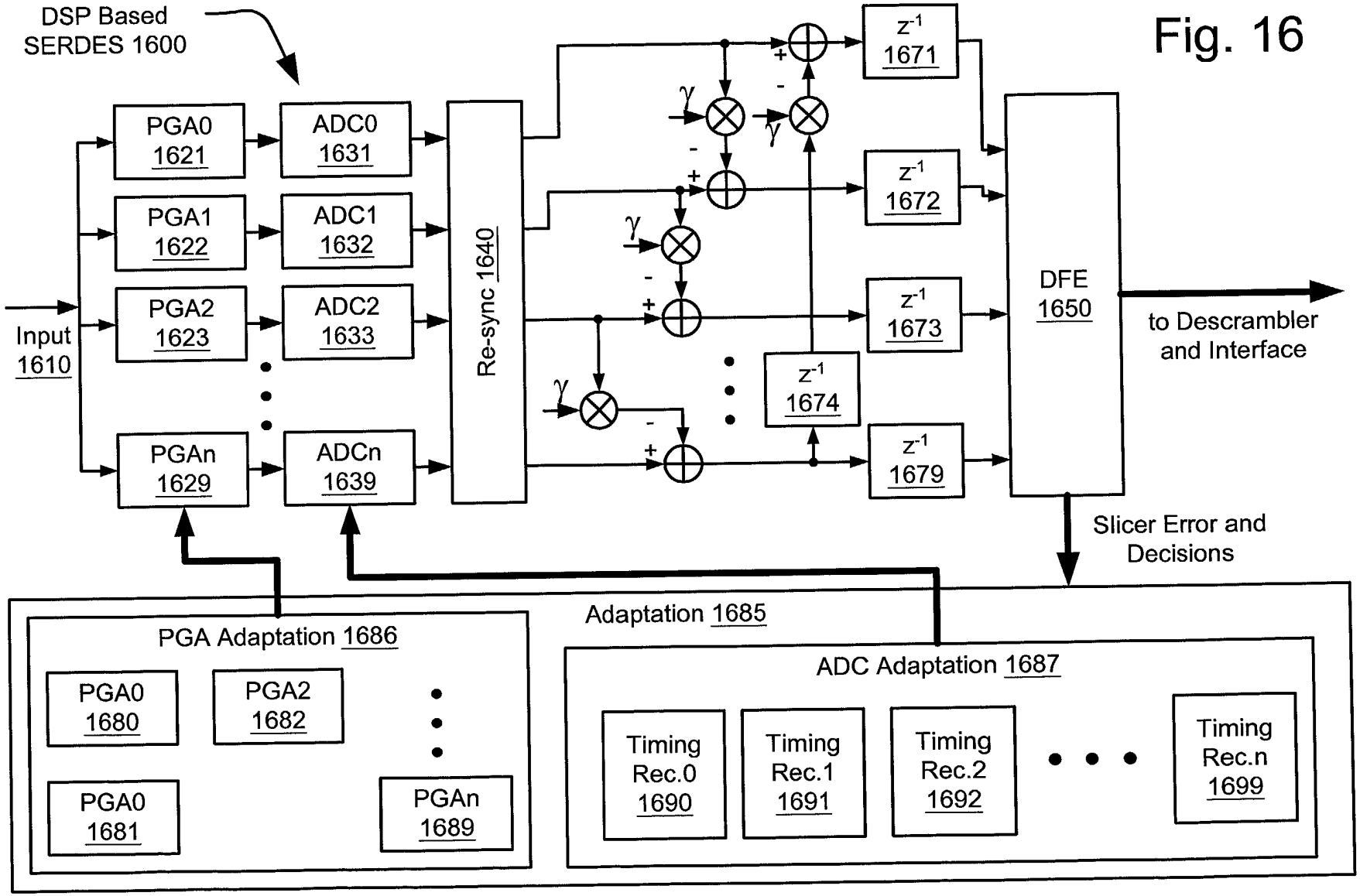

DSP Based
SERDES 1600
PGA0
1621
PGA1
1622
PGA2
1623
PGAn
1629
ADC0
1631
ADC1
1632
ADC2
1633
ADCn
1639
Input
1610
Re-sync 1640
z-1
1671
z-1
1672
z-1
1673
z-1
1674
z-1
1679
DFE
1650
to Descrambler
and Interface
Slicer Error and
Decisions
Adaptation 1685
PGA Adaptation 1686
PGA0
1680
PGA2
1682
PGA0
1681
PGAn
1689
ADC Adaptation 1687
Timing
Rec.0
1690
Timing
Rec.1
1691
Timing
Rec.2
1692
Timing
Rec.n
1699

Fig. 16

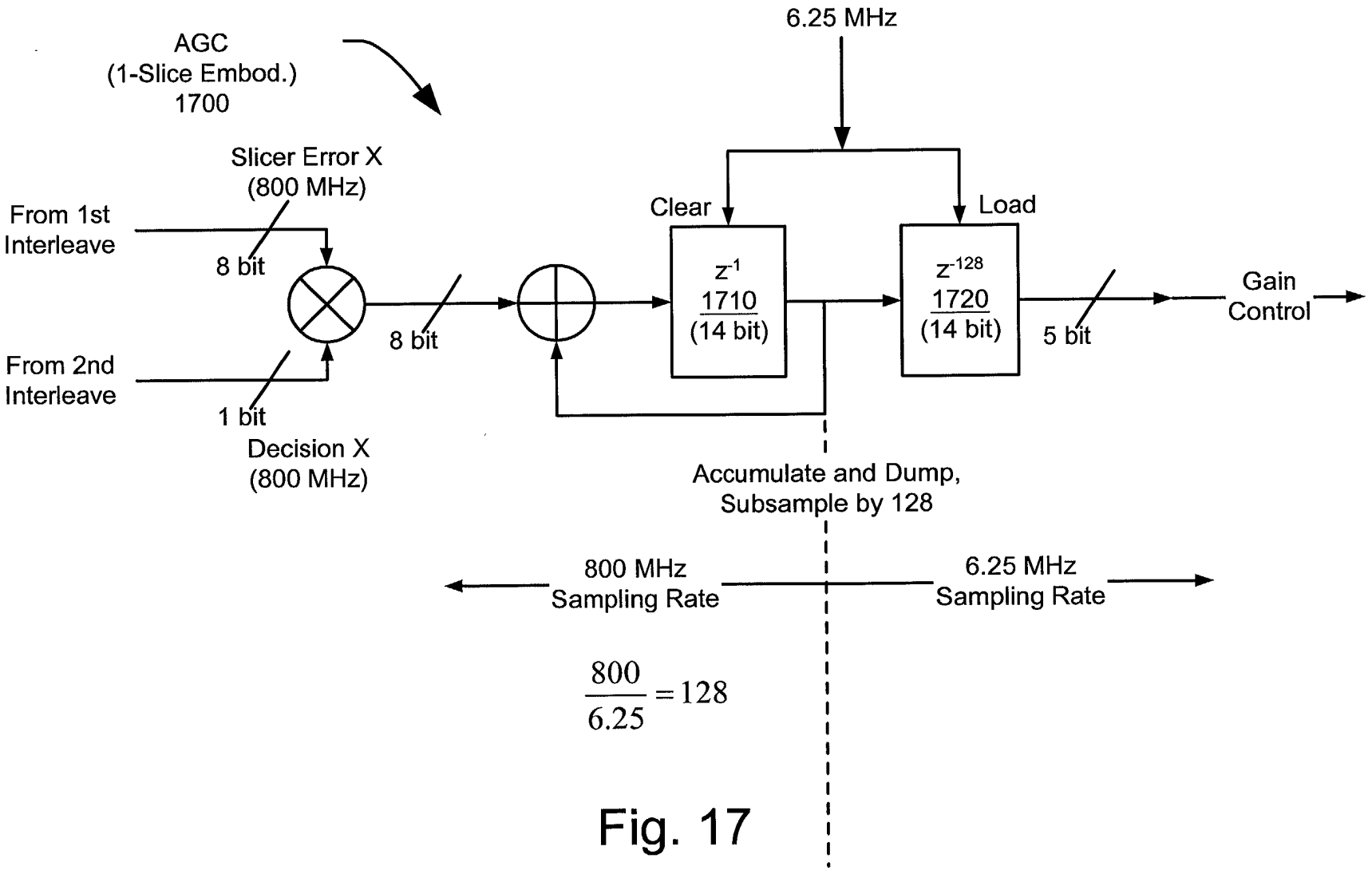
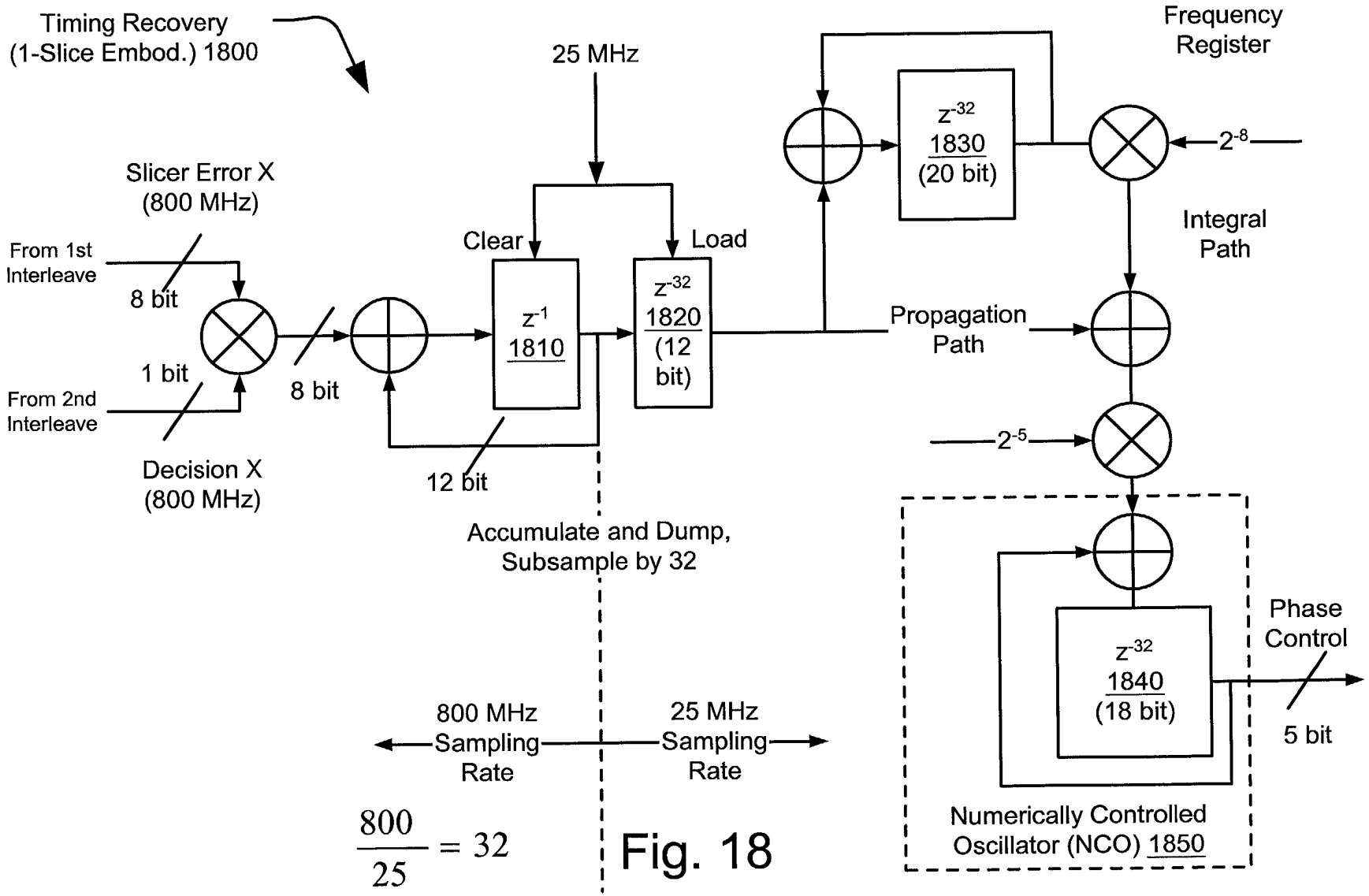

AGC
(1-Slice Embod.)
1700
6.25 MHz
Slicer Error X
(800 MHz)
From 1st
Interleave
8 bit
Clear
Load
z^{-1}
1710
(14 bit)
z^{-128}
1720
(14 bit)
Gain
Control
5 bit
From 2nd
Interleave
8 bit
1 bit
Decision X
(800 MHz)
Accumulate and Dump,
Subsample by 128
800 MHz
Sampling Rate
6.25 MHz
Sampling Rate
$\frac{800}{6.25} = 128$

Fig. 17



$$\frac{800}{25} = 32$$

Fig. 18

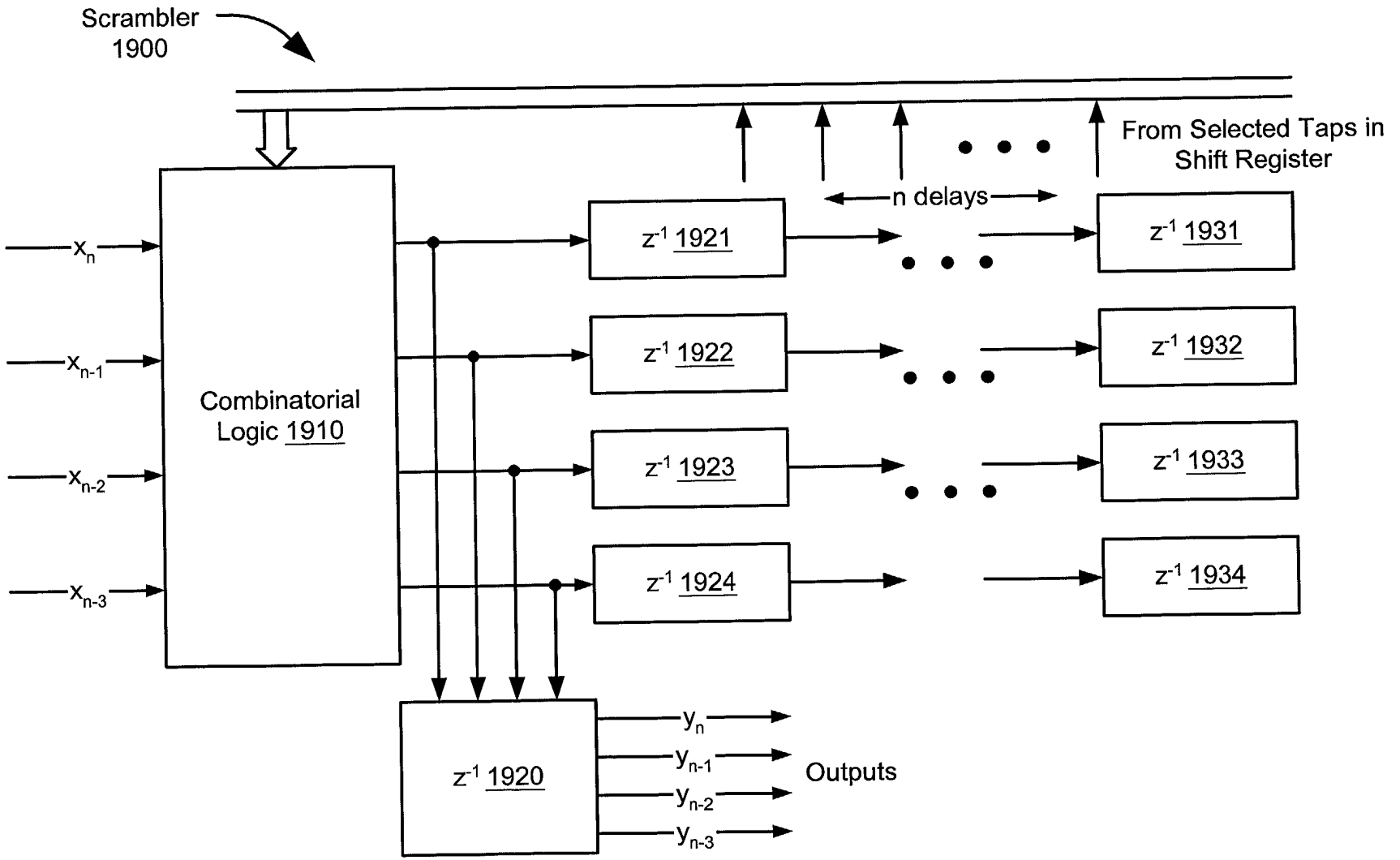

Scrambler
1900
From Selected Taps in
Shift Register
n delays
x_n
x_{n-1}
x_{n-2}
x_{n-3}
Combinatorial
Logic 1910
z^{-1} 1921
z^{-1} 1922
z^{-1} 1923
z^{-1} 1924
z^{-1} 1931
z^{-1} 1932
z^{-1} 1933
z^{-1} 1934
z^{-1} 1920
y_n
y_{n-1}
y_{n-2}
y_{n-3}
Outputs

Fig. 19

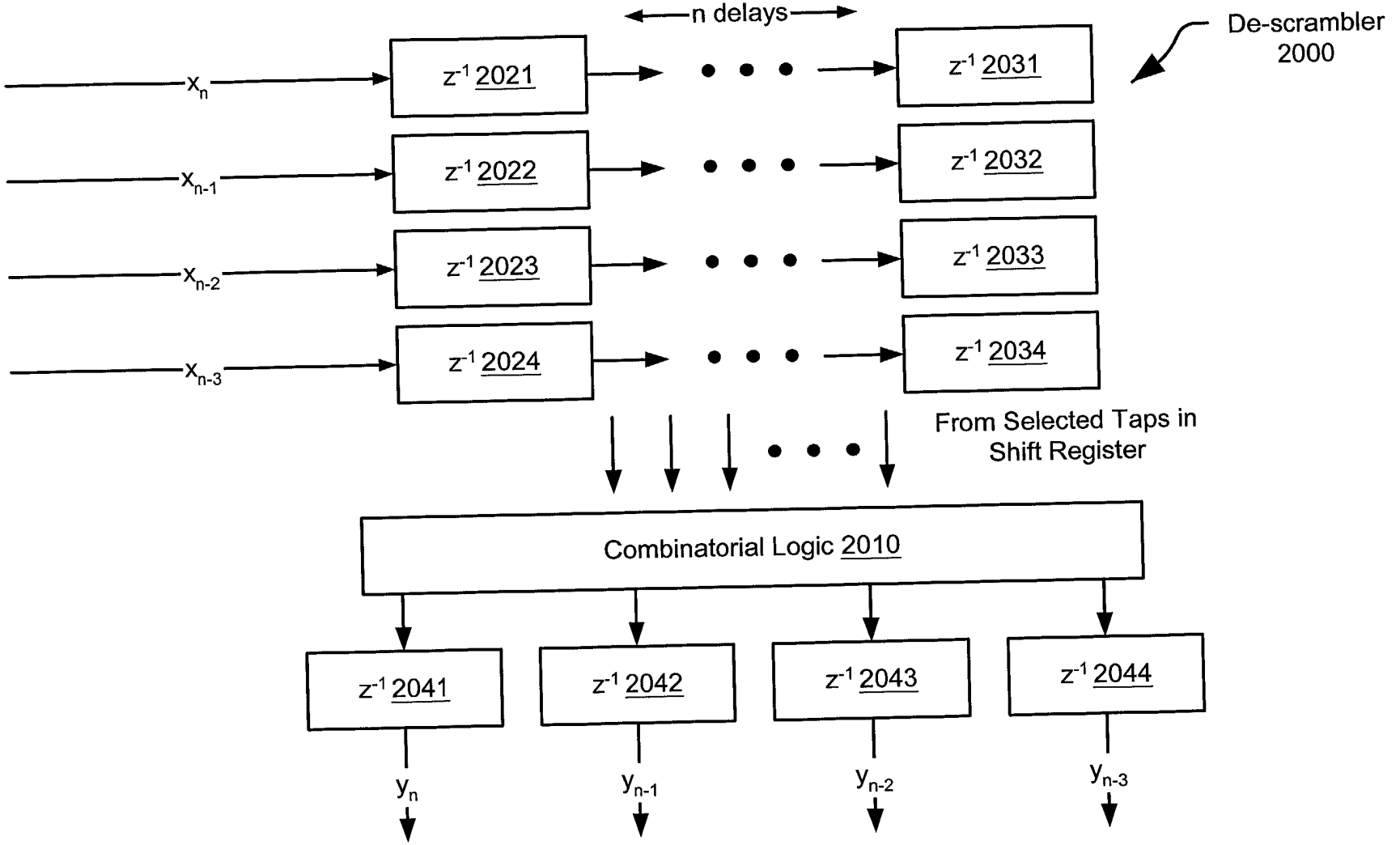

n delays
De-scrambler 2000
x_n
x_{n-1}
x_{n-2}
x_{n-3}
z^{-1} 2021
z^{-1} 2022
z^{-1} 2023
z^{-1} 2024
z^{-1} 2031
z^{-1} 2032
z^{-1} 2033
z^{-1} 2034
From Selected Taps in Shift Register
Combinatorial Logic 2010
z^{-1} 2041
z^{-1} 2042
z^{-1} 2043
z^{-1} 2044
y_n
y_{n-1}
y_{n-2}
y_{n-3}

Fig. 20

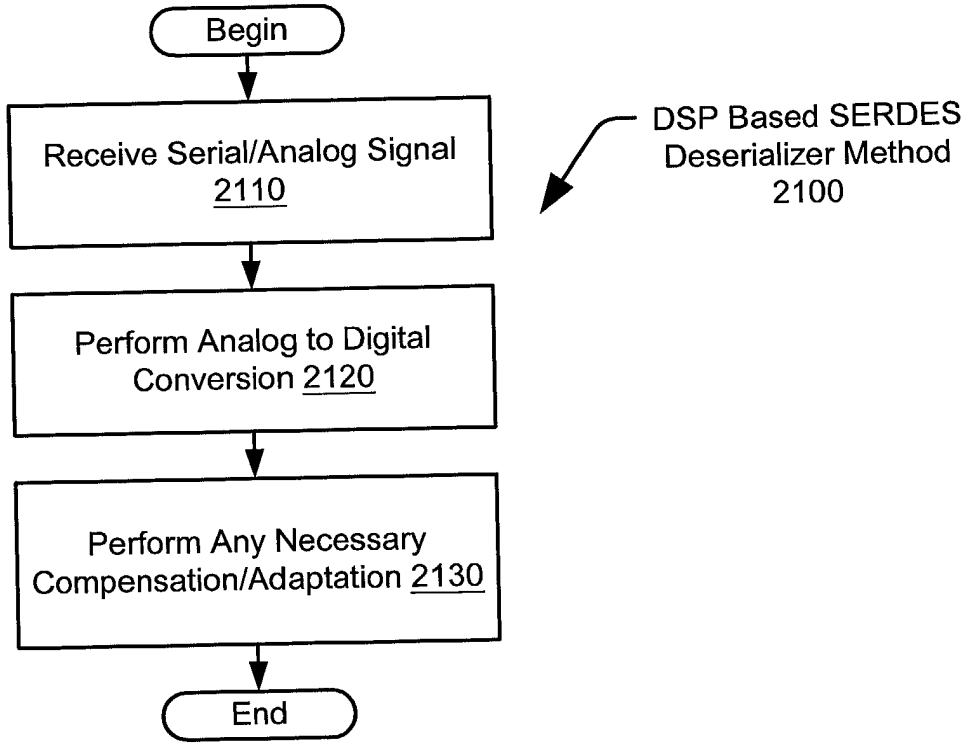

Begin
Receive Serial/Analog Signal 2110
DSP Based SERDES Deserializer Method 2100
Perform Analog to Digital Conversion 2120
Perform Any Necessary Compensation/Adaptation 2130
End

Fig. 21

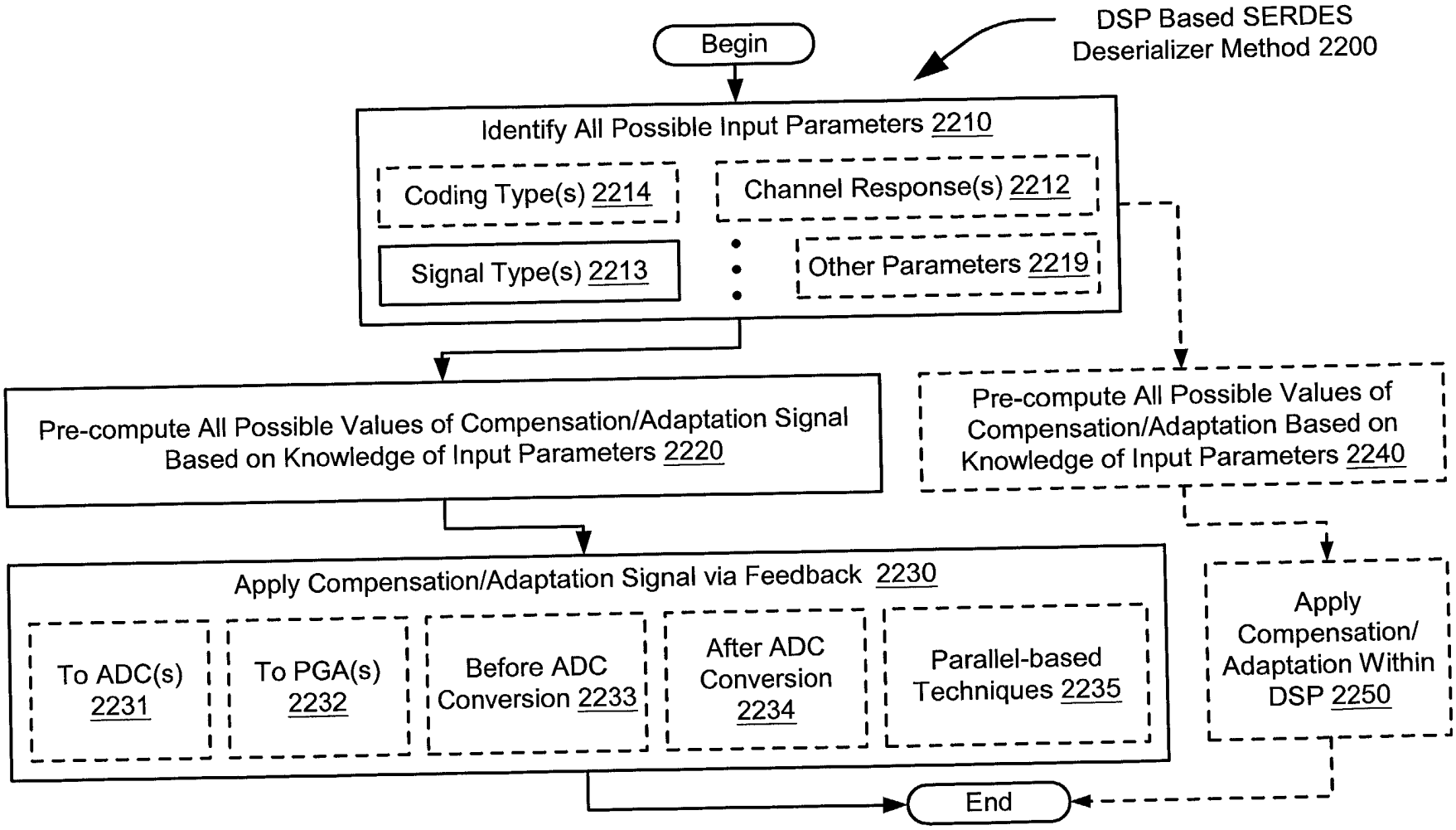

DSP Based SERDES
Deserializer Method 2200
Begin
Identify All Possible Input Parameters 2210
Coding Type(s) 2214
Channel Response(s) 2212
Signal Type(s) 2213
Other Parameters 2219
Pre-compute All Possible Values of Compensation/Adaptation Signal Based on Knowledge of Input Parameters 2220
Pre-compute All Possible Values of Compensation/Adaptation Based on Knowledge of Input Parameters 2240
Apply Compensation/Adaptation Signal via Feedback 2230
To ADC(s) 2231
To PGA(s) 2232
Before ADC Conversion 2233
After ADC Conversion 2234
Parallel-based Techniques 2235
Apply Compensation/ Adaptation Within DSP 2250
End

Fig. 22

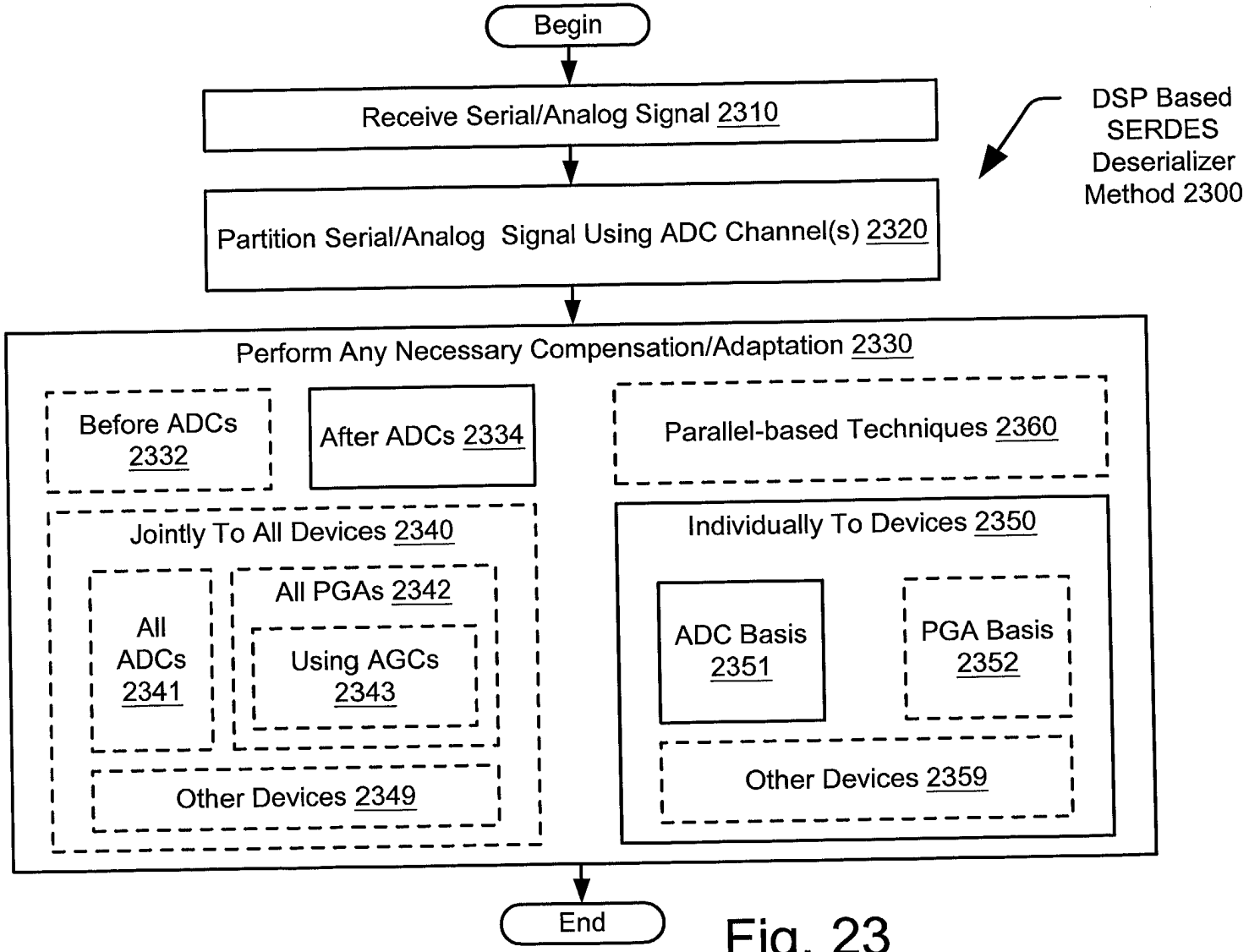

Begin
Receive Serial/Analog Signal 2310
DSP Based SERDES Deserializer Method 2300
Partition Serial/Analog Signal Using ADC Channel(s) 2320
Perform Any Necessary Compensation/Adaptation 2330
Before ADCs 2332
After ADCs 2334
Parallel-based Techniques 2360
Jointly To All Devices 2340
All ADCs 2341
All PGAs 2342
Using AGCs 2343
Other Devices 2349
Individually To Devices 2350
ADC Basis 2351
PGA Basis 2352
Other Devices 2359
End

Fig. 23

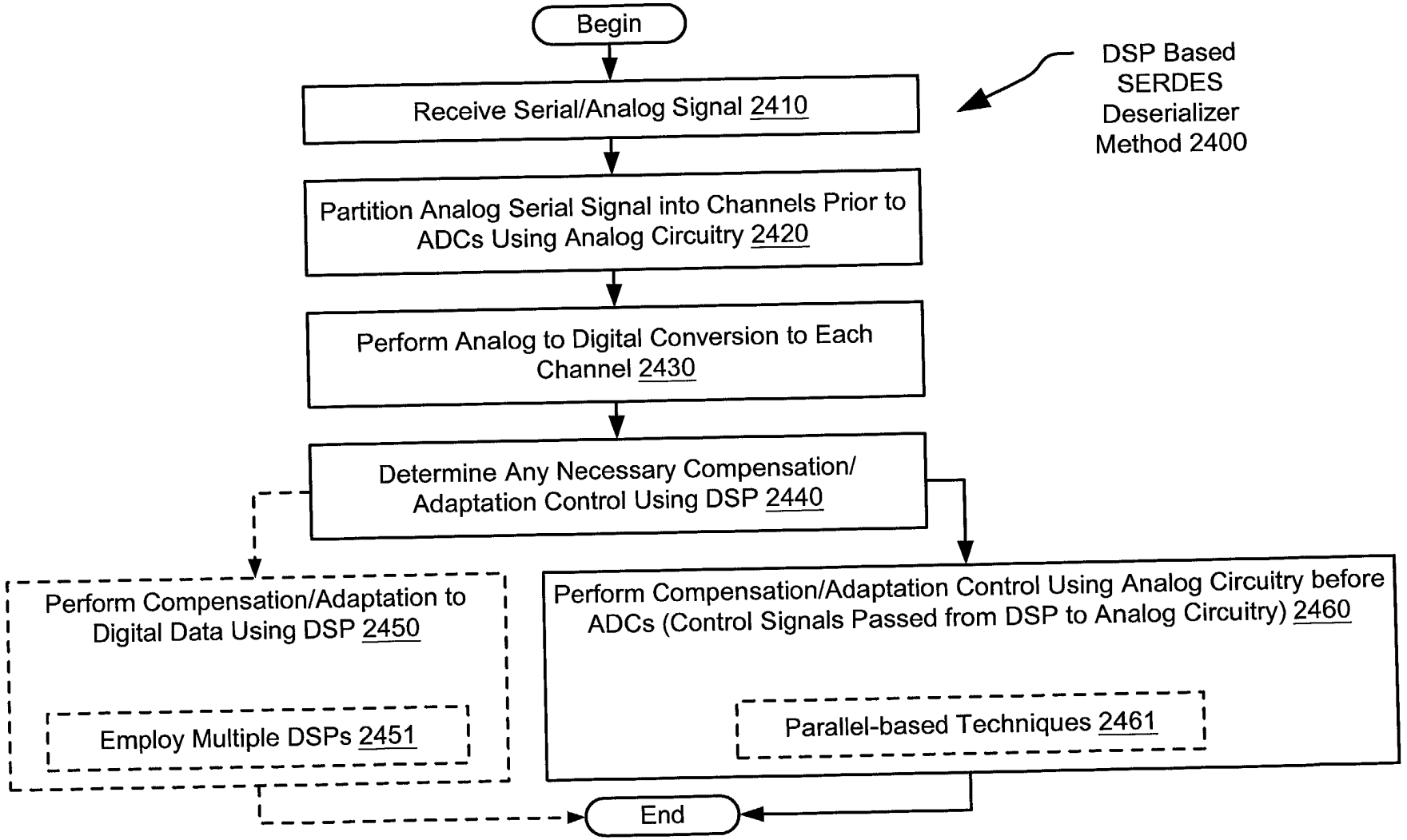

Begin
Receive Serial/Analog Signal 2410
DSP Based SERDES Deserializer Method 2400
Partition Analog Serial Signal into Channels Prior to ADCs Using Analog Circuitry 2420
Perform Analog to Digital Conversion to Each Channel 2430
Determine Any Necessary Compensation/ Adaptation Control Using DSP 2440
Perform Compensation/Adaptation to Digital Data Using DSP 2450
Employ Multiple DSPs 2451
Perform Compensation/Adaptation Control Using Analog Circuitry before ADCs (Control Signals Passed from DSP to Analog Circuitry) 2460
Parallel-based Techniques 2461
End

Fig. 24

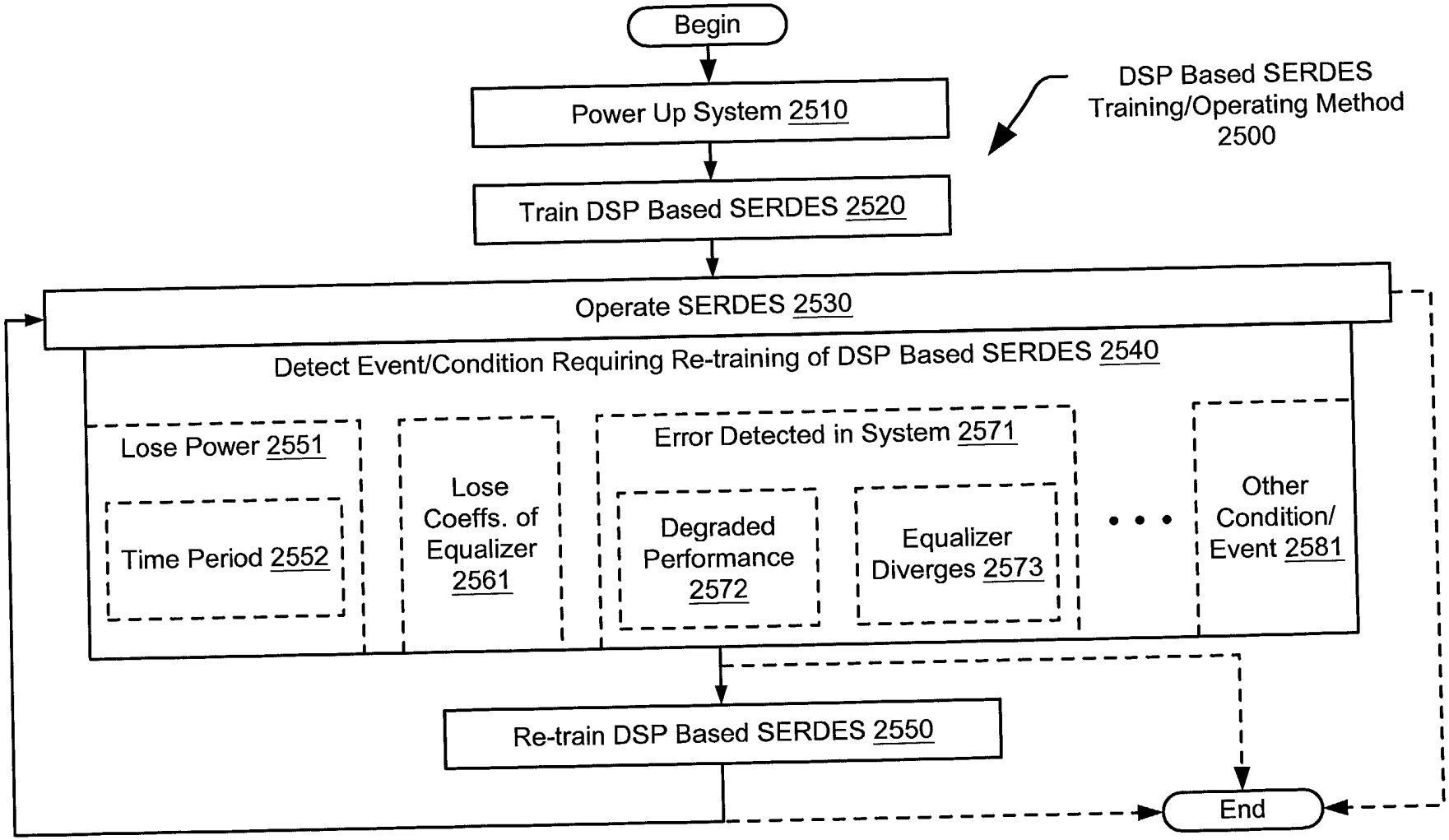

Begin
Power Up System 2510
DSP Based SERDES Training/Operating Method 2500
Train DSP Based SERDES 2520
Operate SERDES 2530
Detect Event/Condition Requiring Re-training of DSP Based SERDES 2540
Lose Power 2551
Time Period 2552
Lose Coeffs. of Equalizer 2561
Error Detected in System 2571
Degraded Performance 2572
Equalizer Diverges 2573
Other Condition/ Event 2581
Re-train DSP Based SERDES 2550
End

Fig. 25

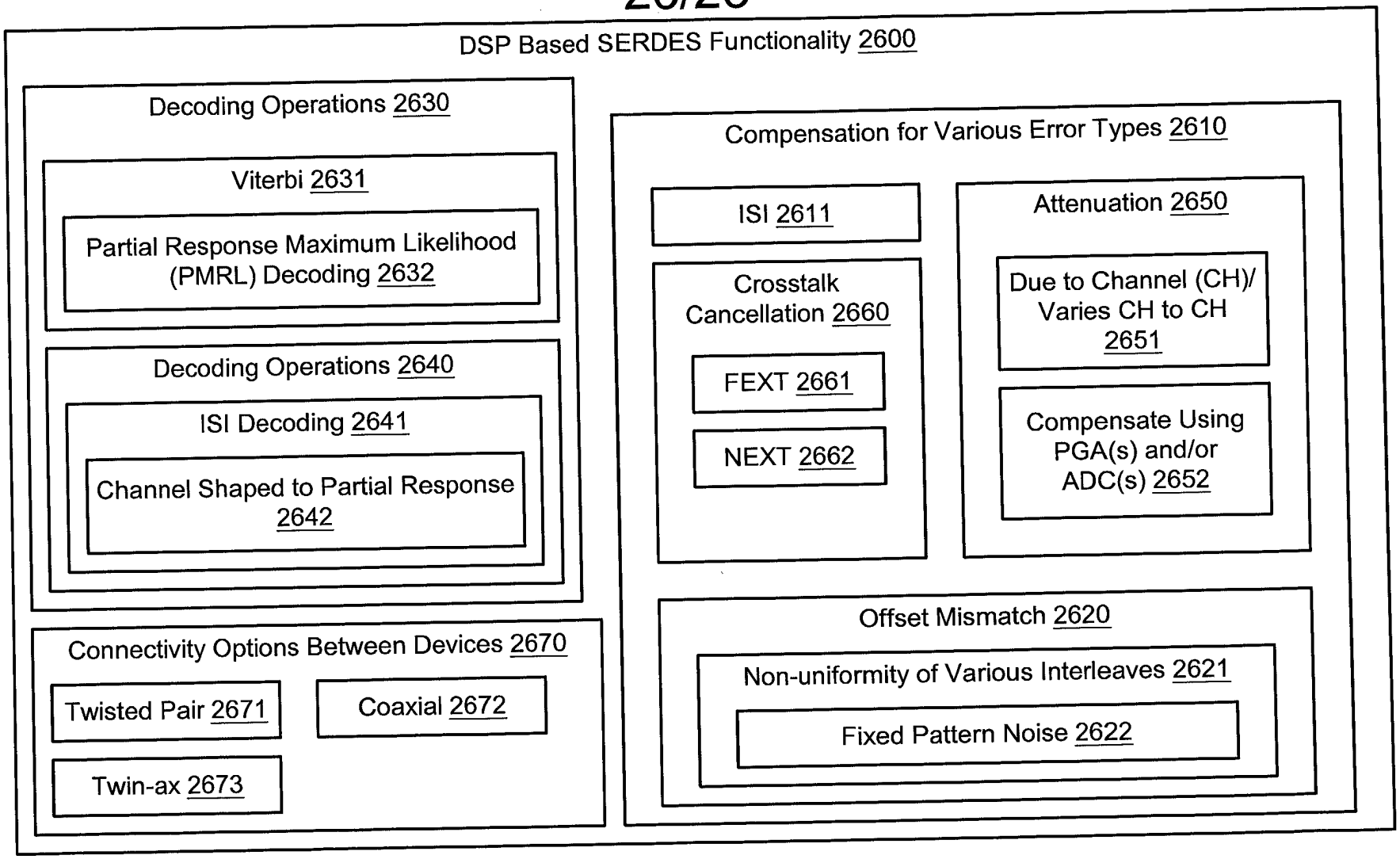

DSP Based SERDES Functionality 2600
Decoding Operations 2630
Viterbi 2631
Partial Response Maximum Likelihood (PMRL) Decoding 2632
Decoding Operations 2640
ISI Decoding 2641
Channel Shaped to Partial Response 2642
Connectivity Options Between Devices 2670
Twisted Pair 2671
Coaxial 2672
Twin-ax 2673
Compensation for Various Error Types 2610
ISI 2611
Crosstalk Cancellation 2660
FEXT 2661
NEXT 2662
Attenuation 2650
Due to Channel (CH)/ Varies CH to CH 2651
Compensate Using PGA(s) and/or ADC(s) 2652
Offset Mismatch 2620
Non-uniformity of Various Interleaves 2621
Fixed Pattern Noise 2622

Fig. 26